What is claimed is:

1. In a process of fabricating a narrow channel width PMOSFET device, the improvement of affecting reduction of negative bias temperature instability by use of F_2 side wall implantation, comprising:

a) forming a shallow trench isolation (STI) region in a substrate;

b) forming a gate on a gate oxide in said substrate;

c) forming a liner layer in said shallow trench isolation region and subjecting said liner layer to oxidation to form a STI liner oxidation layer;

d) implanting F_2 into side walls of said STI liner oxidation layer at a large tilted angle in sufficient amounts to affect reduction of negative bias temperature instability after a high density plasma fill of said STI F_2 implanted liner oxidation layer; and

e) filling the STI F_2 implanted structure from step d) with a high density plasma (HDP) fill to affect reduction of negative bias temperature instability.

2. The process of claim 1 wherein said substrate is Si.

3. The process of claim 2 wherein said liner oxidation layer is SiO_2.

4. The process of claim 2 wherein said liner oxidation layer is SiON.

5. The process of claim 3 wherein said large tilted angle is from about 10 to about 30 degrees with reference to the y axis.

6. The process of claim 4 wherein said large tilted angle is from about 10 to about 30 degrees with reference to the Y axis.

7. The process of claim of 5 wherein said sufficient amount of F_2 is a dose of from about 5 x 10^{12} to about 1x10^{14}cm^2 .

8. The process of claim 6 wherein said sufficient amount of F_2 is a dose of from about 5 x 10^{12} to about 1x10^{14}cm^2 .

9. The process of claim 7 wherein said high density plasma (HDP) fill is a HDP oxide fill.

10. The process of claim 8 wherein said high density plasma (HDP) fill is a HDP oxide fill.